What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

a memory cell array that has a plurality of memory cells arranged in a row direction and a column direction, respectively, each memory cell having a transistor formed with a floating gate between a channel area and a control gate via an insulation film, the control gates of the memory cells in the same row being mutually connected to form common word lines, and drains of the memory cells in the same column being mutually connected to form common bit lines;

word line voltage supply means for selecting the word line connected to the memory cell which is to be programmed with data, and applying a programming gate voltage to the selected word line; and

bit line voltage supply means for selecting the bit line connected to the memory cell which is to be programmed with data, and applying a programming drain voltage to the selected bit line, wherein

the word line voltage supply means is configured to be able to apply gate voltages to the same memory cell such that the gate voltage applied at and after the second time is different from the gate voltage applied at the first time, and

at least one of the word line voltage supply means and the bit line voltage supply means is set to be able to apply a voltage to the same memory cell for a longer application period at the first time than at the second time.

2. The nonvolatile semiconductor memory device according to claim

1, wherein

the word line voltage supply means applies the gate voltages to the same memory cell such that the gate voltage applied at and after the second time is gradually higher than the gate voltage that is applied at the first time.

3. The nonvolatile semiconductor memory device according to claim 2, wherein

the word line voltage supply means applies the gate voltages at and after the second time such that the gate voltage increases by a constant value from the gate voltage applied one time before.

4. The nonvolatile semiconductor memory device according to claim 1, further comprising:

program verification means for verifying a programming state of the memory cell to be programmed with data, wherein

the program verification means verifies the programming state of the memory cell each time after the application of the gate voltage ends.

5. The nonvolatile semiconductor memory device according to claim 4, wherein

at least one of the word line voltage supply means and the bit line voltage supply means does not apply the voltage to the memory cell which the program verification means verifies that the threshold voltage is at a predetermined set value or more.

6. The nonvolatile semiconductor memory device according to claim 1, wherein

the word line voltage supply means selectively applies two or more different voltages to the same memory cell as the gate voltages applied at the first time, thereby to store data of three or more levels to each memory cell.

7. The nonvolatile semiconductor memory device according to claim 1, wherein

at least one of the word line voltage supply means and the bit line voltage supply means applies voltages to the same memory cell such that the voltage application period becomes gradually longer at stages from the second time to a predetermined application time after the third time.

8. The nonvolatile semiconductor memory device according to claim 1, wherein

at least one of the word line voltage supply means and the bit line voltage supply means applies voltages to the same memory cell such that the voltage application period becomes gradually longer at stages from the second time to a predetermined application time after the third time, and that the first application period is equal to the application period at and after the predetermined application time.

9. The nonvolatile semiconductor memory device according to claim

7, wherein

the word line voltage supply means applies the gate voltages to the same memory cell such that the gate voltage applied at and after the second time is gradually higher than the gate voltage that is applied at the first time.

10. The nonvolatile semiconductor memory device according to claim 9, wherein

the word line voltage supply means applies the gate voltages at and after the second time such that the gate voltage increases by a constant value from the gate voltage applied one time before.

11. The nonvolatile semiconductor memory device according to claim 7, further comprising:

program verification means for verifying a programming state of the memory cell to be programmed with data, wherein

the program verification means verifies the programming state of the memory cell each time after the application of the gate voltage ends.

12. The nonvolatile semiconductor memory device according to claim 11, wherein

at least one of the word line voltage supply means and the bit line voltage supply means does not apply the voltage to the memory cell which the program verification means verifies that the threshold voltage is at a predetermined set value or more.

13. The nonvolatile semiconductor memory device according to claim 7, wherein

the word line voltage supply means selectively applies two or more different voltages to the same memory cell as the gate voltages applied at the first time, thereby to store data of three or more levels to each memory cell.

14. The nonvolatile semiconductor memory device according to claim 1, wherein

the word line voltage supply means is configured to be able to adjust the application period at the first time by intermittently applying the same voltage as the gate voltage applied at the first time.

15. The nonvolatile semiconductor memory device according to claim 1, wherein

the word line voltage supply means is configured to be able to apply gate voltages to the same memory cell such that the gate voltage applied at the second time is same as the gate voltage applied at the first time.

16. A nonvolatile semiconductor memory device comprising:

a memory cell array that has a plurality of memory cells arranged in a row direction and a column direction, respectively, each memory cell having a transistor formed with a floating gate between a channel area and a control gate via an insulation film, the control gates of the memory cells in

the same row being mutually connected to form common word lines, and drains of the memory cells in the same column being mutually connected to form common bit lines;

word line voltage supply means for selecting the word line connected to the memory cell which is to be programmed with data, and applying a programming gate voltage to the selected word line; and

bit line voltage supply means for selecting the bit line connected to the memory cell which is to be programmed with data, and applying a programming drain voltage to the selected bit line, wherein

the word line voltage supply means is configured to be able to apply gate voltages to the same memory cell such that the gate voltage applied at and after the second time is different from the gate voltage applied at the first time, the voltage difference between the gate voltage applied at the first time and the gate voltage applied at the second time is set to be different from the voltage difference between the gate voltage applied at the second time and the gate voltage applied at the third time, and the gate voltage applied at and after the third time gradually increases at stages according to the number of times of application.

17. The nonvolatile semiconductor memory device according to claim 16, wherein

at least one of the word line voltage supply means and the bit line voltage supply means applies voltages to the same memory cell such that the first application period is equal to the application period at and after the second application times.

18. The nonvolatile semiconductor memory device according to claim 16, wherein

the word line voltage supply means applies the gate voltages to the same memory cell such that the gate voltage applied at the second time is not higher than the gate voltage applied at the first time.

19. The nonvolatile semiconductor memory device according to claim 16, wherein

the word line voltage supply means applies the gate voltages to the same memory cell such that the increase in the gate voltage applied at and after the third time is gradually made larger than the increase in the gate voltage applied one time before.

20. The nonvolatile semiconductor memory device according to claim 16, further comprising:

program verification means for verifying a programming state of the memory cell to be programmed with data, wherein

the program verification means verifies the programming state of the memory cell each time after the application of the gate voltage ends.

21. The nonvolatile semiconductor memory device according to claim 20, wherein

at least one of the word line voltage supply means and the bit line voltage supply means does not apply the voltage to the memory cell which

the program verification means verifies that the threshold voltage is at a predetermined set value or more.

22. The nonvolatile semiconductor memory device according to claim 16, wherein

the word line voltage supply means selectively applies two or more different voltages to the same memory cell as the gate voltages applied at the first time, thereby to store data of three or more levels to each memory cell.

23. The nonvolatile semiconductor memory device according to claim 16, wherein

the word line voltage supply means is configured to be able to apply gate voltages to the same memory cell such that the gate voltage applied at the second time is same as the gate voltage applied at the first time.

24. A nonvolatile semiconductor memory device comprising:

a memory cell array that has a plurality of memory cells arranged in a row direction and a column direction, respectively, each memory cell having a transistor formed with a floating gate between a channel area and a control gate via an insulation film, the control gates of the memory cells in the same row being mutually connected to form common word lines, and drains of the memory cells in the same column being mutually connected to form common bit lines;

word line voltage supply means for selecting the word line connected

to the memory cell which is to be programmed with data, and applying a programming gate voltage to the selected word line;

bit line voltage supply means for selecting the bit line connected to the memory cell which is to be programmed with data, and applying a programming drain voltage to the selected bit line; and

program verification means for verifying a programming state of the memory cell to be programmed with data, wherein

the word line voltage supply means is configured to be able to apply gate voltages to the same memory cell such that the gate voltage applied at and after the second time is different from the gate voltage applied at the first time, and that the gate voltage applied at and after the second time gradually increases at stages according to the number of times of application, and

the program verification means is set not to verify the programming state after the application of the gate voltage at the first time or from the first time to the predetermined application time.

25. The nonvolatile semiconductor memory device according to claim 24, wherein

the word line voltage supply means continuously applies the gate voltage to the same memory cell from the first time to the predetermined application time.

26. The nonvolatile semiconductor memory device according to claim 24, wherein

at least one of the word line voltage supply means and the bit line voltage supply means applies voltages to the same memory cell such that the first application period is equal to the application period at and after the second application times.

27. The nonvolatile semiconductor memory device according to claim 24, wherein

the word line voltage supply means applies the gate voltages at and after the second time such that the gate voltage increases by a constant value from the gate voltage applied one time before.

28. The nonvolatile semiconductor memory device according to claim 24, wherein

at least one of the word line voltage supply means and the bit line voltage supply means does not apply the voltage to the memory cell which the program verification means verifies that the threshold voltage is at a predetermined set value or more.

29. The nonvolatile semiconductor memory device according to claim 24, wherein

the word line voltage supply means selectively applies two or more different voltages to the same memory cell as the gate voltages applied at the first time, thereby to store data of three or more levels to each memory cell.

30. The nonvolatile semiconductor memory device according to claim 24, wherein

the word line voltage supply means is configured to be able to apply gate voltages to the same memory cell such that the gate voltage applied at the second time is same as the gate voltage applied at the first time.